Category-IV

Pool of Generic Electives offered by Department of Electronic Science

GENERIC ELECTIVES (GE-2A): **Digital System Design**

Credit distribution, Eligibility and Pre-requisites of the Course

Course title & Code	Credits	Credit distribution of the course			Eligibility criteria	Pre-requisite of the course	Department offering the course
		Lecture	Tutorial	Practical/ Practice			
Digital System Design	4	3	0	1	Class 12th Pass with PCM or Physics, Comp. Sc. & Maths.	Nil	Electronic Science

Learning Objectives

In addition to familiarization with the combinational and sequential circuits, students will be adept in using simulation of digital circuits on software, which is in high demand, for designing combinational or sequential circuits. As there are lot of industrial and research-based job opening in the area, the course offers a hands-on in designing digital systems on hardware and testing with a holistic approach to the subject, making students ready for the industry or research

Learning outcomes

After completion of the course, students will be able to-

Understand and represent numbers in powers of base and concepts of Boolean algebra.
Understand basic logic gates and minimization techniques.
Analyze and design combinatorial circuits.
Analyze and design sequential circuits.

SYLLABUS

UNIT – I Number Systems and Boolean Algebra (09 Hours)

Number System and Boolean algebra: Decimal, Binary, Hexadecimal, Octal, BCD, Conversions, Complements (1's and 2's), Signed and unsigned numbers, addition and subtraction, Gray Code. Boolean algebra- Positive and negative logic. Boolean laws, De Morgan's theorems, simplification of Boolean expressions-SOP and POS

UNIT – II Logic Gates and Minimization (12 Hours)

Logic gates and Karnaugh map: Logic gates- basic logic gates-AND, OR, NOT, logic symbol and truth table. Derived logic gates (NAND, NOR, XOR & XNOR). Universal property of NOR and NAND gates. K-map minimization of 3 and 4 variable functions/expressions.

UNIT – III Combinational Circuits (12 Hours)

Combinational logic analysis and design: Multiplexers and Demultiplexers, Adder (half and full), Subtractor (half and full), Parallel adder/subtractor, Encoder and Decoder, Understanding VHDL program of a Full Adder and 3 to 8 decoder

UNIT – IV Flip Flops and Counters (12 Hours)

Sequential logic design: Latch, Flip flop, S-R FF , J-K FF, T and D type FFs, clocked FFs, registers, Counters (synchronous and asynchronous, ring and Johnson)

Practical component (if any) - Digital System Design Lab – 30 Hours

(Hardware and Circuit Simulation Software)

To verify and design AND, OR, NOT and XOR gates using NAND gates.
2. Design a Half and Full Adder.
3. Design a Half and Full Subtractor.
4. Implement Boolean functions using 8X1 and 16X1 Multiplexers.
5. Implement Boolean functions using decoder.
6. Implement an encoder.
7. Study of counters using dedicated counter ICs.
8. Study of registers (SISO, SIPO, PISO and PIPO) using universal shift register IC.

Note: Students shall sincerely work towards completing all the above listed practicals for this course. In any circumstance, the completed number of practicals shall not be less than seven.

Essential/recommended readings

1. M. Morris Mano Digital System Design,Pearson Education Asia,(Fourth Edition)
2. Thomas L. Flyod, Digital Fundamentals, Pearson Education Asia (1994)
3. W. H. Gothmann, Digital Electronics: An Introduction To Theory And Practice, Prentice Hall of India(2000)
4. R. L. Tokheim, Digital Principles, Schaum_s Outline Series, Tata McGraw- Hill (1994)